REMARKS

Claims 1-4 were previously withdrawn. Claim 8 was previously cancelled.

In this paper the amendments that were previously presented in the Amendment After Final Rejection that was mailed on 4 December 2003 are repeated for the Examiner's convenience. Consequently, claims 5, 6, 7, 9, 10, and 14 are amended. No new subject matter is added.

In addition to the preceding amendments, new claims 18-26 are added. No new subject matter is present.

Claims 5-7 and 9-26 remain in the case for consideration. Allowance of claims 5-7 and 9-26 is respectfully requested in light of the following remarks.

Statutory Period for Reply

In response to the Final Office Action that was mailed on 7 October 2003, an Amendment After Final Rejection was deposited on 4 December 2003, within two months of the final rejection, using proper Certificate of Mailing procedures as defined under 37 CFR 1.8. Consequently, the shortened statutory period for reply expired on the date that the Advisory Action was mailed (January 20, 2004). See MPEP 706.07(f). As a result, this RCE is submitted with the fee for a one month extension of time.

Claim Rejections – 35 USC § 112, first paragraph

Claims 14-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. It is alleged that there is no description in the disclosure for the feature recited in claim 14 of an impurity implantation region with a top surface of the impurity implantation region that is larger than a bottom surface. The applicants disagree.

To the contrary, possession may be shown *in a variety of ways* including description of an actual reduction to practice, *or* by showing that the invention was "ready for patenting" *such as by the disclosure of drawings . . .*, *or* by describing distinguishing identifying characteristics (see MPEP 2163(I); emphasis added). An applicant may show possession of an invention by *disclosure of drawings* (see MPEP 2163(II)(A)(3)(a); emphasis added).

The original disclosure is replete with drawings that show an impurity implantation region with a top surface that is larger than a bottom surface (see, e.g, element 54, FIG. 5a; element 64, FIG. 6a; element 74, FIG. 7a).

Claim Rejections – 35 USC § 112, second paragraph

Claims 6, 11, (and apparently 15 as well) are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In particular, it is alleged that it is unclear as to what is meant by the term "line width." The applicants disagree.

The line widths of active regions, impurity implantation regions, and gates are all indicated to be important values (page 5, lines 23-24). FIGS. 3 and 4 illustrate a gate 36 with line width W2 (page 2, line 27). FIGS. 5a and 5b illustrate a gate 56 with line width W3 and an active region with line width F (page 6, lines 5-6). Like FIGS. 5a and 5b, FIGS. 6a and 6b illustrate a gate 56 with line width W3 and an active region with line width F (page 7, lines 12-14). Like FIGS. 5a and 5b, FIGS. 7a and 7b illustrate a gate 56 with line width W3 and an active region with line width F (page 7, lines 21-23).

To the contrary, it is abundantly clear from the disclosure what the term "line width" means.

Claim Rejections – 35 USC § 103

Claims 5-7 and 9-17, are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,668,021 to Subramanian et al., (hereafter, 'Subramanian') in view of Applicant Admitted Prior art (hereafter, 'AAPA'). It is alleged that Subramanian and AAPA teach that the line width of the first surface of the semiconductor substrate is equal to the line width of the impurity implantation region. The applicants disagree.

Claim 5 is amended to recite, *inter alia*, an impurity implantation region of impurities of a second conductivity type formed in the channel region, the impurity implantation region separated from the source region and the drain region; the impurity implantation region comprising a depletion channel of the second conductivity type, the impurity implantation region including a first surface of the semiconductor substrate, wherein a line width of the first surface is equal to a line width of the impurity implantation region.

These amendments are fully supported by the original disclosure (see, e.g., FIG. 7a). The terms "first sector" and "second sector" were removed to increase the clarity of the claims. The term "surface region" was replaced with "surface," also to increase the clarity of the claim.

The words of the claims must be given their plain meaning (MPEP 2111.01). Claim 5 recites an impurity implantation region formed ***in*** the semiconductor substrate, and that the impurity region ***includes*** a first surface of the semiconductor substrate (emphasis added).

Obviously, since the impurity implantation region and the first surface are distinctly claimed, they must be two distinct entities. According to Merriam Webster's College Dictionary (10^{th} ed., 1996) a "surface" is the *exterior or upper boundary of an object or body*. Thus, it is plain that the recited first surface of the semiconductor substrate is the interface between the impurity implantation region 74 and the gate insulating layer 34 (see FIG. 7a).

With reference to Subramanian FIGS. 2-7, it is clear that Subramanian does not teach or suggest an impurity implantation region 24 that includes a surface of the semiconductor substrate where the line width of the surface equals the line width of the impurity implantation region. Any other proposed interpretation is contrary to the plain meaning of the claim. The AAPA does not teach the features of the recited impurity implantation region or the recited first surface of the semiconductor substrate either.

Consequently, a *prima facie* case of obviousness is not established because Subramanian/AAPA fail to teach each and every feature recited in claim 5 (MPEP 2143.03).

Regarding claim 10, it recites, *inter alia*, that the impurity implantation region comprises a first surface region that functions as a depletion channel and that occupies ***the entire top surface of the semiconductor substrate within the lateral extent of the impurity implantation region*** (emphasis added).

The words of the claims must be given their plain meaning (MPEP 2111.01). The "***entire top surface*** of the semiconductor substrate ***within the lateral extent of the impurity implantation region***" plainly defines the boundaries of the top surface of the semiconductor substrate (emphasis added).

To the contrary, the Subramanian's egg-shaped region 24 does not have a surface region that occupies the entire top surface of the semiconductor substrate within the lateral extent of the impurity implantation region. Rather, Subramanian's egg-shaped region 24 occupies *only a tiny portion of the entire top surface of the semiconductor substrate that is within the lateral extent of the impurity implantation region* (see Subramanian FIGS. 2-7; emphasis added).

Pending claims must also be interpreted consistently with the specification (see, e.g., MPEP 2111). The Examiner's interpretation is inconsistent with the specification (see, e.g, FIG. 7a). The AAPA does not teach the recited features of the claimed impurity implantation region either.

Consequently, a *prima facie* case of obviousness is not established because Subramanian/AAPA fail to teach all the features recited in claim 10 (MPEP 2143.03).

Regarding claim 14, it recites, *inter alia*, that the impurity implantation region comprises *a first surface region* that functions as a depletion channel and *that occupies the entire top surface of the semiconductor substrate within the first sector* (emphasis added). The claim also recites that the lateral extent of the impurity implantation region is coextensive with that of the first sector.

To the contrary, Subramanian does not teach or suggest an egg-shaped region 24 that occupies ***the entire top surface of the semiconductor substrate within the first sector*** (see FIGS. 2-7; emphasis added). The Examiner's interpretation is contrary to the plain meaning of the words of the claim (see MPEP 2111.01). The Examiner's interpretation is also inconsistent with the specification (see MPEP 2111 and FIG. 7a). The AAPA does not teach the recited features of the claimed impurity implantation region either.

Consequently, a *prima facie* case of obviousness is not established because Subramanian/AAPA fail to teach each and every feature recited in claim 14 (MPEP 2143.03).

Further in regard to claims 5, 10, and 14, the claims are amended to recite that the gate has a narrowest width that is greater than a line width (or lateral extent) of the impurity implantation region. This amendment is fully supported by FIG. 7a of the original disclosure.

Subramanian and AAPA do not teach or suggest this feature. In particular, it is seen in Subramanian FIG. 2 that the lateral extent of the gate electrode is defined by the size of opening 18 (column 3, lines 20-22). The narrowest width of the opening 18 is not greater than the lateral extent of the impurity implantation region 24, thus the narrowest width of the gate electrode 26 cannot be larger than the lateral extent of the impurity implantation region 24 (see FIG. 7).

New Claims 18-26

New claims 18-26 are directed at the improved input/output terminal structure of a semiconductor device, and are fully supported by the original disclosure.

Claim 18 recites, *inter alia*, an open drain transistor and an enhancement transistor, the gate of the enhancement transistor having a length greater than the length of the gate of the open drain transistor. This feature is supported by the original disclosure at, e.g., page 11, lines 3-5. Subramanian does not disclose this feature.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 5-7 and 9-26 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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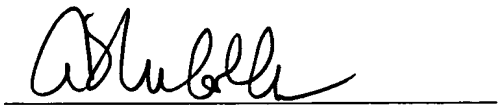

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